

STAR Trigger Level 0 Configurations– Run 2006

Last update: 12th May 2006

TCU Input Bit Lists

Bit	Set 1 – Minimum Bias & Central Research 11_ld301_ctb_zdc.rbt Used in these Tier1 files: 040126	Set 2 – Primary Data Taking 11_ld301_2006.rbt Used in these Tier1 files: 060307 060313 060316 060318 060323 060326 060328 060509	Set 3 – Pedestal and Test Data Taking 11_ld301_pedestal_2006.rbt Used in these Tier1 files: 060316_pedestal 060509_pedestal
0	CTB Multiplicity > th0	MTD trigger	Req. bit 0
1	CTB Multiplicity > th1	FPD1	Req. bit 1
2	CTB Multiplicity > th2	FPD2	Req. bit 2
3	BBC TAC diff in window	EMC Total Energy Sum	Detector ID bit 0
4	ZDC TAC diff in window	J/Ψ trigger	Detector ID bit 1
5	BBC East _{small} ADC > th	BEMC HT.TP>th	Detector ID bit 2
6	BBC West _{small} ADC > th	BEMC HT>th2	Detector ID bit 3
7	ZDC East ADC > th0	BEMC Jet Patch: 1	Unused
8	ZDC West ADC > th0	BEMC Jet Patch: 2	Unused
9	ZDC East TAC in window	EEMC HT.TP>th	Unused
10	ZDC West TAC in window	EEMC HT>th2	Unused
11	ZDC E+W attenuated ADC sum > th	EEMC Jet Patch: 1	Unused
12	Zero Bias bit	EEMC Jet Patch: 2	Unused
13	Blue bunch filled	Prescaled minimum bias	Minimum Bias
14	Yellow bunch filled	Minimum bias	Zero Bias
15	Special Trigger Flag (Off)	Zero Bias	Random Bit

NOTES:

- Please see the documentation for the individual RBT files on the STAR Trigger Web Pages at http://www.star.bnl.gov/STAR/html/trg_1/TSL/index.html in the Software section for a description of what these bits mean.
- In Set 1 if the Special Trigger Flag is ON then the TCU input bits have the following definitions:

Bit	Special Requests
0	Req. bit 0
1	Req. bit 1
2	Req. bit 2
3	Detector ID bit 0
4	Detector ID bit 1
5	Detector ID bit 2
6	Detector ID bit 3
7	Random Bit
8	
9	
10	
11	
12	
13	
14	
15	Special Trigger Flag (On)

Tier1 Files

041026

BBC	Good ADC values are summed and the sums are compared to thresholds for East and West separately. The fastest good TAC is found for East and West separately, and their difference is calculated. “Killer Bits” are used in the ADC sum logic.
ZDC	ADC values are compared to thresholds. A window is put on each TAC value, and in parallel the TAC difference is calculated “Killer Bits” are used in the ADC-threshold and TAC-window logic The SMD data is just recorded
CTB	The ADC values are all summed. The UPC-topology logic runs in parallel
BEMC/EEMC	Jet patch energy sums and high towers are compared to 3 thresholds. The results are combined for the Barrel and Endcap separately. J/Ψ detection logic is based on the West half of the barrel only. The back-to-back detection logic is not implemented The adjacent jet patch logic can use the Barrel, Endcap or both.
FPE/FPW	High-tower algorithms are now in use: 3 thresholds are applied to each ADC. The results are combined for East and West separately.
L1	Set 1 - Minimum Bias and Central Research (see TCU Input Bits List above)

060307

BBC	LUTS at input to final VTX DSM (VT201) are changed from 1-to-1 maps to files that are read in.
ZDC	This allows the user to re-map the TAC difference bits to a range useful for the scalers. Otherwise, same as 040126
MTD	ADC values are compared to a threshold. The threshold bits are combined to indicate a particle passing through all 3 layers of the detector. NOTE: A bug was fixed in this algorithm: the MTD data is now passed from MD001 to channel 4 of ZD101, instead of channel 2, to be consistent with the way this system is actually cabled.
CTB	Same as 040126
BEMC/EEMC	High towers, trigger patch energies and jet patch energy sums are compared to 3 thresholds. The result for each trigger patch is combined with its associated high tower. The results are combined for the Barrel and Endcap separately. J/Ψ detection logic is based on the barrel only. The jet patch energies are summed to give the total energy in the Barrel, Endcap and the full calorimeter. The 3 total energy measurements are each compared to a threshold
FPE/FPW	A sum algorithm is used to measure the total energy in each FPD-East module and each FPD++ module. The energies are compared to thresholds
L1	Set 2 – Primary Data Taking (see TCU Input Bits List above)

060313

BBC	Same as 060307
ZDC	
MTD	Same as 060307
CTB	Same as 040126
BEMC/EEMC	Same as 060307
FPE/FPW	The 2006 version of the FP201 algorithm is installed to process the new FPD++ data.
L1	Set 2 – Primary Data Taking (see TCU Input Bits List above)

NOTE: The size of the minimum bias prescale register was increased from 5 to 8 bits. There were no changes to any of the input or output data bits.

060316

BBC	Same as 060307
ZDC	
MTD	Same as 060307
CTB	The last 8 DSMS in this system have been removed leaving just the first 8
BEMC/EEMC	The input to EM201 from EE101 is zeroed out in the EM201 LUT
FPE/FPW	The FPE North-South layer 0 DSMS have switched from a 15-channel to a 16-channel sum algorithm.
L1	Same as 060313

060316 – Pedestal/Test Version

BBC	Same as 060307
ZDC	
MTD	Same as 060307
CTB	Same as 060316
BEMC/EEMC	Same as 060307 (i.e. nothing is zeroed out)
FPE/FPW	Same as 060316
L1	Set 3 – Pedestal and Test Data Taking (see TCU Input Bits List above)

060318 – NOTE: This Tier1 file is being used as a testing ground. It is being modified to fix problems as they are identified. The table below lists the current state of this Tier1 file.

BBC	Same as 060307
ZDC	
MTD	Same as 060307
CTB	Same as 060316
BEMC/EEMC	EE101 is no longer zeroed out at the input to EM201, the layer-2 EMC DSM Bits 0-8 of channel 2 have been set to 5 (i.e. the expected pedestal value) in the input to EE101. This corresponds to bits 16-24 out of EE002, which is one of the jet patch energies The 4 MSB of channel 4 have been zeroed out of the EE101 input. This corresponds to the TP and HT.TP bits of the EE004 output Bits 10 and 11 of channel 3 have been zeroed out in the input to BE101. This corresponds to bits 26 and 27 out of BE003, which are the HT bits from the second trigger patch.
FPE/FPW	FW004 has been switched from the algorithm that sums 2 groups of 8 channels to the old one (still used by FE004) that sums 2 groups of 7 channels. FE101 and FE102 have switched to the masked sum already used by FW101 and FW102
L1	Same as 060313

060323

BBC	Same as 060307
ZDC	
MTD	Same as 060307
CTB	Same as 060316
BEMC/EEMC	The HT bits from the second patch in BE003 are no longer zeroed out at the input to BE101. Otherwise, same as final version of 060318
FPE/FPW	Same as final version of 060318
L1	Same as 060313

060326

BBC	ZDC and Small-tile BBC TAC difference bits are swapped on the cable that goes from the
ZDC	“Vertex” DSM board (VT201) to the Scaler Source Patch Panel, otherwise same as 060307
MTD	Same as 060307
CTB	Same as 060316
BEMC/EEMC	Same as 060323
FPE/FPW	Same as 060323
L1	Same as 060313

060328

BBC	Same as 060307
ZDC	
MTD	Same as 060307
CTB	Same as 060316
BEMC/EEMC	Same as 060307, i.e. nothing is zeroed out anymore
FPE/FPW	Same as 060323
L1	Same as 060313

060509

BBC	Same as 060307
ZDC	
MTD	Same as 060307
CTB	Same as 060313, i.e. last 8 DSMs have been restored
BEMC/EEMC	Same as 060307
FPE/FPW	FPE Top/Bottom DSMs (FE008,9,10,11 and FE102) have been removed
L1	FE102 outputs have been zeroed out at the input to FP201 (channels 2 and 3), otherwise same as 060313

060509 – Pedestal/Test Version

BBC	Same as 060307
ZDC	
MTD	Same as 060307
CTB	Same as 060313, i.e. last 8 DSMs have been restored
BEMC/EEMC	Same as 060307
FPE/FPW	FPE Top/Bottom DSMs (FE008,9,10,11 and FE102) have been removed
L1	Same as 060316_Pedestal